**CHAPTER TWO**

**CURRENT DIRECTION**

The particles that carry charge through wires in a circuit are mobile electrons. The electric field direction within a circuit is by definition the direction that positive test charges are pushed. Thus, these negatively charged electrons move in the direction opposite the electric field. But while electrons are the charge carriers in metal wires, the charge carriers in other circuits can be positive charges, negative charges or both. In fact, the charge carriers in semiconductors, street lamps and fluorescent lamps are simultaneously both positive and negative charges traveling in opposite directions.

Ben Franklin, who conducted extensive scientific studies in both static and current electricity, envisioned positive charges as the carriers of charge. As such, an early convention for the direction of an electric current was established to be in the direction that positive charges would move. The convention has stuck and is still used today.



The **direction of an electric current** is by convention the direction in which a positive charge would move. Thus, the current in the external circuit is directed away from the positive terminal and toward the negative terminal of the battery. Electrons would actually move through the wires in the opposite direction. Knowing that the actual charge carriers in wires are negatively charged electrons may make this convention seem a bit odd and outdated.

**DC CIRCUITS**

**KIRCHHOFF’S LAWS**

Kirchhoff’s laws were first introduced in 1847 by the German physicist Gustav Robert Kirchhoff (1824–1887). These laws are formally known as Kirchhoff’s current law (KCL) and Kirchhoff’s voltage law (KVL).

**Kirchhoff’s current law (KCL): S**tates that the algebraic sum of currents entering a node (or a closed boundary) is zero.

 Mathematically, KCL implies that



where *N* is the number of branches connected to the node and *in* is the *n*th current entering (or leaving) the node. By this law, currents entering a node may be regarded as positive, while currents leaving the node may be taken as negative or vice versa.

Consider the node in Figure shown below. Applying KCL gives



since currents *i*1*, i*3, and *i*4 are entering the node, while currents *i*2 and *i*5 are leaving it. By rearranging the terms, we get

*i*1 + *i*3 + *i*4 = *i*2 + *i*5-------------------------(1)

Equation (1) is an alternative form of KCL:

The sum of the currents entering a node is equal to the sum of the currents leaving the node.

A simple application of KCL is combining current sources in parallel. The combined current is the algebraic sum of the current supplied by the individual sources. For example, the current sources shown in Figure 1 (a) can be combined as in Figure 1(b). The combined or equivalent current source can be found by applying KCL to node *a*.

*IT* + *I*2 = *I*1 + *I*3

*IT* = *I*1 − *I*2 + *I*3



Figure 1(a)



Figure 1(b)

A circuit cannot contain two different currents, *I*1 and *I*2, in series, unless *I*1 = *I*2; otherwise KCL will be violated.

**Kirchhoff’s voltage law (KVL)**: States that the algebraic sum of all voltages around a closed path (or loop) is zero.

Expressed mathematically, KVL states that



Where *M* is the number of voltages in the loop (or the number of branches in the loop) and *vm* is the *m*th voltage.

**Note:** Kirchhoff’s second law is based on the principle of conservation of energy:

 To illustrate KVL, consider the circuit in Figure 2. The sign on each voltage is the polarity of the terminal encountered first as we travel around the loop. We can start with any branch and go around the loop either clockwise or counterclockwise.

Suppose we start with the voltage source and go clockwise around the loop as shown; then voltages would be −*v*1*,*+*v*2*,*+*v*3*,*−*v*4, and +*v*5, in that order. For example, as we reach branch 3, the positive terminal is met first; hence we have+*v*3*.*

For branch 4, we reach the negative terminal first; hence, −*v*4. Thus, KVL yields

−*v*1 + *v*2 + *v*3 − *v*4 + *v*5 = 0-------------(2)



Figure 2: A single-loop circuit illustrating KVL.

which may be interpreted as

*v*2 + *v*3 + *v*5 = *v*1 + *v*4--------------------(3)

which may be interpreted as

sum of the voltage drops=sum of the voltage rises

 When voltage sources are connected in series, KVL can be applied to obtain the total voltage. The combined voltage is the algebraic sum of the voltages of the individual sources. For example, for the voltage sources shown in Figure 3(a), the combined or equivalent voltage source in Figure 3(b) is obtained by applying KVL.

−*Vab* + *V*1 + *V*2 − *V*3 = 0

(or)

*Vab* = *V*1 + *V*2 − *V*3-------------------------(4)



1. (b)

Figure 3: Voltage sources in series: (a) original circuit, (b) equivalent circuit.

Example:

For the circuit in Figure (a), find voltages *v*1 and *v*2.



**Solution:**

To find *v*1 and *v*2, we apply Ohm’s law and Kirchhoff’s voltage law. Assume that current *i* flows through the loop as shown in Fig. 2.21(b). From Ohm’s law,

*v*1 = 2*i, v*2 = −3*i-----------*(1)

Applying KVL around the loop gives

−20 + *v*1 − *v*2 = 0------------(2)

Substituting *i* in Eq. 1 finally gives

*v*1 = 8 V*, v*2 = −12 V

Exercise: Find *v*1 and *v*2 in the circuit of Figure shown below.

Answer: 12 V, −6 V.



Problem: Determine *vo* and *i* in the circuit shown in below.



Solution:



We apply KVL around the loop as shown in Fig. 2.23(b). The result is

−12 + 4*i* + 2*vo* − 4 + 6*i* = 0 (1)

Applying Ohm’s law to the 6-*\_* resistor gives

*vo* = −6*i* (2)

Substituting Eq. (2) into Eq. (1) yields

−16 + 10*i* − 12*i* = 0 ⇒ *i* = −8 A

and *vo* = 48 V.

**Exercise:** Find *vx* and *vo* in the circuit of Figure shown below.

Answer: 10 V, −5 V.



**Problem:** Find current *io* and voltage *vo* in the circuit shown in Figure below.

****

**Solution:**

Applying KCL to node *a*, we obtain

3 + 0*.*5*io* = *io*  ⇒ *io* = 6 A

For the 4Ωresistor, Ohm’s law gives

*vo* = 4*io* = 24 V

**Exercise:** Find *vo* and *io* in the circuit of Figure shown in below.

**Answer:** 8 V, 4 A.



**Problem:** Find the currents and voltages in the circuit shown in Figure (a) below.



(a)

**Solution:**



We apply Ohm’s law and Kirchhoff’s laws. By Ohm’s law,

*v*1 = 8*i*1*, v*2 = 3*i*2*, v*3 = 6*i*3 (1)

Since the voltage and current of each resistor are related by Ohm’s

law as shown, we are really looking for three things: *(v*1*, v*2*, v*3*)* or *(i*1*, i*2*, i*3). At node *a*, KCL gives

*i*1 − *i*2 − *i*3 = 0 (2)

Applying KVL to loop 1 as in Figure (b),

−30 + *v*1 + *v*2 = 0

We express this in terms of *i*1 and *i*2 as in Eq. (2.8.1) to obtain

−30 + 8*i*1 + 3*i*2 = 0

or

 (3)

Applying KVL to loop 2,

−*v*2 + *v*3 = 0 ⇒ *v*3 = *v*2 (4)

as expected since the two resistors are in parallel. We express *v*1 and *v*2 in terms of *i*1 and *i*2 as in Eq. (1). Equation (4) becomes

6*i*3 = 3*i*2 ⇒ *i*3 = *i*2/2 (5)

Substituting Eqs. (3) and (5) into (2) gives



or

*i*2 = 2 A. From the value of *i*2, we now use Eqs. (1) to (5) to obtain

*i*1 = 3 A*, i*3 = 1 A*, v*1 = 24 V*, v*2 = 6 V*, v*3 = 6 V.

**Exercise:** Find the currents and voltages in the circuit shown in Figure below.

**Answer:** *v*1 = 3 V, *v*2 = 2 V, *v*3 = 5 V, *i*1 = 1*.*5 A, *i*2 = 0*.*25 A,

*i*3 =1.25 A.



**SERIES RESISTORS AND VOLTAGE DIVISION:**

The need to combine resistors in series or in parallel occurs so frequently that it warrants special attention. The process of combining the resistors is facilitated by combining two of them at a time. With this in mind, consider the single-loop circuit of Figure 4. The two resistors are in series, since the same current *i* flows in both of them. Applying Ohm’s law to each of the resistors, we obtain

*v*1 = *iR*1*, v*2 = *iR*2 (1)

If we apply KVL to the loop (moving in the clockwise direction), we have

−*v* + *v*1 + *v*2 = 0 (2)



Figure 4: A single-loop circuit with two resistors in series.

Combining Eqs. (1) and (2), we get

*v* = *v*1 + *v*2 = *i(R*1 + *R*2*)* (3)

or



Notice that Eq. (3) can be written as

*v* = *iR*eq (4)

implying that the two resistors can be replaced by an equivalent resistor *R*eq; that is,

*R*eq = *R*1 + *R*2 (5)



Figure: Equivalent circuit of the Figure 4 circuit.

Note: The equivalent resistance of any number of resistors connected in series is the sum of the individual resistances.

For *N* resistors in series then,



To determine the voltage across each resistor in Figure 4.



Notice that the source voltage *v* is divided among the resistors in direct proportion to their resistances; the larger the resistance, the larger the voltage drop. This is called the **principle of****voltage division**, and the circuit in Figure 4 is called a **voltage divider**.

In general, if a voltage divider has*N* resistors (*R*1*,R*2*, . . . , RN)* in series with the source voltage *v*, the *n*th resistor (*Rn*) will have a voltage drop of



**PARALLEL RESISTORS AND CURRENT DIVISION:**

Consider the circuit in Figure 5, where two resistors are connected in parallel and therefore have the same voltage across them. From Ohm’s law,

*v* = *i*1*R*1 = *i*2*R*2

(or)

 (1)



Figure 5: Two resistors in parallel.

Applying KCL at node *a* gives the total current *i* as

*i* = *i*1 + *i*2 (2.34)

Substituting Eq. (2.33) into Eq. (2.34), we get

(2)

where *R*eq is the equivalent resistance of the resistors in parallel:

 (6)

Or



**Or**

****

The equivalent resistance of two parallel resistors is equal to the product of their resistances divided by their sum.

if N resisters are in parallel, the equivalent resistance is



Given the total current *i* entering node *a* in Figure 5, how do we obtain current *i*1 and *i*2? We know that the equivalent resistor has the same voltage, or

 (3)

Combining Eqs. (1) and (3) results in



which shows that the total current *i* is shared by the resistors in inverse proportion to their resistances. This is known as the **principle of current division,** and the circuit in Figure 5, is known as a **current divider.** Notice that the larger current flows through the smaller resistance.



Figure 6: Equivalent circuit to figure 5.

**Problem:** Find *R*eq for the circuit shown in Figure.



**Solution:** To get *R*eq, we combine resistors in series and in parallel. The 6Ωand 3 Ωresistors are in parallel, so their equivalent resistance is



(The symbol “║” is used to indicate a parallel combination.) Also, the 1Ω and 5Ωresistors are in series; hence their equivalent resistance is

1Ω+ 5 Ω= 6 Ω

Thus the circuit shown above is reduced to that in Figure (a).



In Figure (a), we notice that the two 2Ω resistors are in series, so the equivalent resistance is

2Ω+ 2Ω= 4Ω

This 4Ωresistor is now in parallel with the 6Ωresistor in Figure (a); their equivalent resistance is

****

The circuit in Figure (a) is now replaced with that in Figure (b). In Figure (b), the three resistors are in series. Hence, the equivalent resistance for the circuit is



****

**Exercise:** By combining the resistors in Figure shown below, find *R*eq.



**Answer:** 6Ω

**Problem:** Calculate the equivalent resistance *Rab* in the circuit in Figure (a) below.

****

Figure (a)

**Solution:**

The 3Ωand 6Ωresistors are in parallel because they are connected to the same two nodes *c* and *b*. Their combined resistance is

****

Similarly, the 12 Ωand 4 Ωresistors are in parallel since they are connected to the same two nodes *d* and *b*. Hence

****

Also the 1 Ωand 5Ωresistors are in series; hence, their equivalent resistance is



With these three combinations, we can replace the circuit in Figure (a) with that in Figure (b).



Figure (b)

In figure (b) 3 Ω in parallel with 6 Ω gives 2 Ω. This 2 Ωequivalent resistance is now in series with the 1 Ω resistance to give a combined resistance of 1 Ω +2 Ω= 3 Ω. Thus, we replace the circuit in Figure (b) with that in Figure (c).



Figure (c)

In Figure (c), we combine the 2 Ωand 3 Ωresistors in parallel to get

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This 1.2 Ωresistor is in series with the 10 Ωresistor, so that

****

**NODAL ANALYSIS:**

Nodal analysis provides a general procedure for analyzing circuits using node voltages as the circuit variables. Choosing node voltages instead of element voltages as circuit variables is convenient and reduces the number of equations one must solve simultaneously.

 In nodal analysis, we are interested in finding the node voltages. Given a circuit with n nodes without voltage sources, the nodal analysis of the circuit involves taking the following three steps.

**Steps to Determine Node Voltages:**

1. Select a node as the reference node. Assign voltages *v*1*, v*2*, . . . , vn*−1 to the remaining *n* − 1 nodes. The voltages are referenced with respect to the reference node.

2. Apply KCL to each of the *n* − 1 non-reference nodes. Use Ohm’s law to express the branch currents in terms of node voltages.

3. Solve the resulting simultaneous equations to obtain the unknown node voltages.

**We shall now explain and apply these three steps.**

**The first step** in nodal analysis is selecting a node as the **reference or datum node.** The reference node is commonly called the **ground**since it is assumed to have zero potential. A reference node is indicated by any of the three symbols in Figure 7. The type of ground in Figure 7(b) is called a **chassis ground**and is used in devices where the case, enclosure, or chassis acts as a reference point for all circuits. When the potential of the earth is used as reference, we use the **earth ground**in Figure 7(a) or (c). We shall always use the symbol in Figure 7(b).



Figure 7: Common symbols for indicating a reference node.



Figure 7(a)



Figure 7(b)

Figure 7 (a) & (b) Typical circuit for nodal analysis.

**As the second step:** we apply KCL to each non-reference node in the circuit. To avoid putting too much information on the same circuit, the circuit in Figure 7(a) is redrawn in Figure 7(b), where we now add *i*1*, i*2, and *i*3 as the currents through resistors *R*1*, R*2, and *R*3, respectively.

At node 1, applying KCL gives

*I*1 = *I*2 + *i*1 + *i*2 (1)

At node 2,

*I*2 + *i*2 = *i*3 (2)

We now apply Ohm’s law to express the unknown currents *i*1*, i*2, and *i*3 in terms of node voltages. The key idea to bear in mind is that, since resistance is a passive element, by the passive sign convention, current must always flow from a higher potential to a lower potential.

 We now apply Ohm’s law to express the unknown currents *i*1*, i*2, and *i*3 in terms of node voltages.

We can express this principle as

(3)



 (4)



Substituting Eq. (4) in Eqs. (1) and (2) results, respectively, in

 (5)

 (6)

**As the third step:** to obtain the node voltages *v*1 and *v*2 using any standard method, such as the substitution method, the elimination method, Cramer’s rule, or matrix inversion. To use either of the last two methods. From eq (5) and (6), we can write as matrix form



Problem 1: Calculate the node voltages in the circuit shown in Fig. 3.3(a).



**Solution:**

****

Figure: circuit for analysis

Notice how the currents are selected in the above diagram for the application of KCL. Except for the branches with current sources, the labeling of the currents is arbitrary but consistent. (By consistent, we mean that if, for example, we assume that *i*2 enters the 4*\_*resistor from the left-hand side, *i*2 must leave the resistor from the right-hand side.) The reference node is selected, and the node voltages *v*1 and *v*2 are now to be determined.

At node 1, applying KCL and Ohm’s law gives



Multiplying each term in the last equation by 4, we obtain

20 = *v*1 − *v*2 + 2*v*1

or

3*v*1 − *v*2 = 20 (1)

At node 2, we do the same thing and get



Multiplying each term by 12 results in

3*v*1 − 3*v*2 + 120 = 60 + 2*v*2

or

−3*v*1 + 5*v*2 = 60 (2)

Now we have two simultaneous Eqs. (1) and (2). We can solve the equations using any method and obtain the values of *v*1 and *v*2.

**Method 1:**

Using the elimination technique, we add Eqs. (1) and (2).

4*v*2 = 80 \_⇒ *v*2 = 20 V

Substituting *v*2 = 20 in Eq. (1) gives

3*v*1 − 20 = 20 \_⇒ *v*1 =40/3 = 13*.*33 V.

**Method 2:**

To use Cramer’s rule, we need to put Eqs. (1) and (2) in matrix form as



The determinant of the matrix is

****

We now obtain *v*1 and *v*2 as



If we need the currents, we can easily calculate them from the values of the nodal voltages.



**Problem 2:** Determine the voltages at the nodes in Figure(a).

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Figure (a): original circuit

**Solution:**

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Figure (b): circuit for analysis

The circuit in this example has three non-reference nodes, unlike the previous example which has two non-reference nodes. We assign voltages to the three nodes as shown in Figure (b) and label the currents.

At node 1,

****

Multiplying by 4 and rearranging terms, we get

3*v*1 − 2*v*2 − *v*3 = 12 (1)

At node 2,

****

Multiplying by 8 and rearranging terms, we get

−4*v*1 + 7*v*2 − *v*3 = 0 (2)

At node 3,



Multiplying by 8, rearranging terms, and dividing by 3, we get

2*v*1 − 3*v*2 + *v*3 = 0 (3)

We have three simultaneous equations to solve to get the node voltages *v*1*, v*2, and *v*3. We shall solve the equations in two ways.

**Method 1:**

Using the elimination technique, we add Eqs. (1) and (3).

5*v*1 − 5*v*2 = 12

 (4)

Adding Eqs. (2) and (3) gives

−2*v*1 + 4*v*2 = 0 \_⇒ *v*1 = 2*v*2 (5)

Substituting Eq. (5) into Eq. (4) yields

2*v*2 − *v*2 = 2*.*4 \_⇒ *v*2 = 2*.*4*, v*1 = 2*v*2 = 4*.*8 V

From Eq. (3), we get

*v*3 = 3*v*2 − 2*v*1 = 3*v*2 − 4*v*2 = −*v*2 = −2*.*4 V

Thus,

*v*1 = 4*.*8 V*, v*2 = 2*.*4 V*, v*3 = −2*.*4 V

**Method 2:** To use Cramer’s rule, we put Eqs. (1) to (3) in matrix form.



From this, we obtain



where ∆*,* ∆1*,* ∆2, and ∆3 are the determinants to be calculated as follows. As explained in Appendix A, to calculate the determinant of a 3 by 3 matrix, we repeat the first two rows and cross multiply.



= 21 − 12 + 4 + 14 − 9 − 8 = 10

Similarly, we obtain







Thus, we find







**Exercise:** Find the voltages at the three non-reference nodes in the circuit shown below.

**Answer:** *v*1 = 80 V*, v*2 = −64 V*, v*3 = 156 V.



**Exercise:** Obtain the node voltages in the circuit shown in.

**Answer:** *v*1 = −2 V*, v*2 = −14 V.



**NODAL ANALYSIS WITH VOLTAGE SOURCES**

We now consider how voltage sources affect nodal analysis. We use the circuit in Figure shown below for illustration. Consider the following two possibilities.

****

**CASE 1:1** If a voltage source is connected between the reference node and a non-reference node, we simply set the voltage at the non-reference node equal to the voltage of the voltage source. In Figure above, for example,

*v*1 = 10 V (1)

Thus our analysis is somewhat simplified by this knowledge of the voltage at this node.

**CASE 2:** If the voltage source (dependent or independent) is connected between two non-reference nodes, the two non-reference nodes form a *generalized node* or *supernode*; we apply both KCL and KVL to determine the node voltages.

A **supernode** is formed by enclosing a (dependent or independent) voltage source connected between two non-reference nodes and any elements connected in parallel with it.

In the above circuit, nodes 2 and 3 form a supernode. We analyze a circuit with supernodes using the same three steps mentioned in the previous section except that the supernodes are treated differently. Why? Because an essential component of nodal analysis is applying KCL, which requires knowing the current through each element. There is no way of knowing the current through a voltage source in advance. However, KCL must be satisfied at a supernode like any other node. Hence, at the supernode in the above circuit,

*i*1 + *i*4 = *i*2 + *i*3 (2)

or

****

To apply Kirchhoff’s voltage law to the supernode in above circuit, we redraw the circuit as shown in Fig. 8. Going around the loop in the clockwise direction gives

−*v*2 + 5 + *v*3 = 0 \_⇒ *v*2 − *v*3 = 5 (3)

From Eqs. (1), (2), and (3), we obtain the node voltages.



Figure 8: applying KVL to a supernode

**Problem:** For the circuit shown in Figure shown below, find the node voltages.



**Solution:**

The supernode contains the 2-V source, nodes 1 and 2, and the 10Ωresistor. Applying KCL to the supernode as shown in Fig. 9 (a) gives

2 = *i*1 + *i*2 + 7

Expressing *i*1 and *i*2 in terms of the node voltages



or

*v*2 = −20 − 2*v*1 (1)

To get the relationship between *v*1 and *v*2, we apply KVL to the circuit in Fig. 9(b). Going around the loop, we obtain

**** (2)

From Eqs. (1) and (2), we write

*v*2 = *v*1 + 2 = −20 − 2*v*1

or

3*v*1 = −22 \_⇒ *v*1 = −7*.*333 V

and *v*2 = *v*1 +2 = −5*.*333 V. Note that the 10Ωresistor does not make any difference because it is connected across the supernode.

****

Figure 9: Applying: (a) KCL to the supernode, (b) KVL to the loop.

**Exercise:** Find *v* and *i* in the circuit shown below.

**Answer:** −0*.*2 V, 1.4 A.

****

**Problem:** Find the node voltages in the circuit.

****

**Solution:**

Nodes 1 and 2 form a supernode; so do nodes 3 and 4. We apply KCL to the two supernodes as in Fig. 10(a). At supernode 1-2,

*i*3 + 10 = *i*1 + *i*2

Expressing this in terms of the node voltages,



or

5*v*1 + *v*2 − *v*3 − 2*v*4 = 60 (1)

At supernode 3-4,



or

4*v*1 + 2*v*2 − 5*v*3 − 16*v*4 = 0 (2)



Figure 10: Applying: (a) KCL to the two supernodes, (b) KVL to the loops.

We now apply KVL to the branches involving the voltage sources as shown in Fig. 10(b). For loop 1,

 (3)

For loop 2,

−*v*3 + 3*vx* + *v*4 = 0

But *vx* = *v*1 − *v*4 so that

3*v*1 − *v*3 − 2*v*4 = 0 (4)

For loop 3,

*vx* − 3*vx* + 6*i*3 − 20 = 0

But 6*i*3 = *v*3 − *v*2 and *vx* = *v*1 − *v*4*.* Hence

−2*v*1 − *v*2 + *v*3 + 2*v*4 = 20 (5)

6*v*1 − *v*3 − 2*v*4 = 80 (6)

and

6*v*1 − 5*v*3 − 16*v*4 = 40 (7)

Equations (4), (6), and (7) can be cast in matrix form as







and *v*2 = *v*1−20 = 6*.*667 V. We have not used Eq. (5); it can be used to cross check results.

**MESH ANALYSIS**

A mesh is a loop which does not contain any other loops within it.

Mesh analysis provides another general procedure for analyzing circuits, using mesh currents as the circuit variables. Using mesh currents instead of element currents as circuit variables is convenient and reduces the number of equations that must be solved simultaneously.

**Steps to determine Mesh Currents:**

1. Assign mesh currents *i*1*, i*2*, . . . , in* to the *n* meshes.

2. Apply KVL to each of the *n* meshes. Use Ohm’s law to express the voltages in terms of the mesh currents.

3. Solve the resulting *n* simultaneous equations to get the mesh currents.

**NOTE:** Nodal analysis applies KCL to find unknown voltages in a given circuit, while mesh analysis applies KVLto find unknown currents.

**Problems:** For the circuit in below, find the branch currents *I*1*, I*2, and *I*3 using mesh analysis.



**Solution:**

We first obtain the mesh currents using KVL. For mesh 1,

−15 + 5*i*1 + 10*(i*1 − *i*2*)* + 10 = 0

or

3*i*1 − 2*i*2 = 1 (1)

For mesh 2,

6*i*2 + 4*i*2 + 10*(i*2 − *i*1*)* − 10 = 0

or

*i*1 = 2*i*2 – 1 (2)

**METHOD 1:** Using the substitution method, we substitute Eq. (2) into Eq. (1), and write

6*i*2 − 3 − 2*i*2 = 1 \_⇒ *i*2 = 1 A

From Eq. (2), *i*1 = 2*i*2 − 1 = 2 − 1 = 1 A. Thus,

*I*1 = *i*1 = 1 A*, I*2 = *i*2 = 1 A*, I*3 = *i*1 − *i*2 = 0

**METHOD 2:** To use Cramer’s rule, we cast Eqs. (1) and (2) in matrix form as

****

We obtain the determinants







Thus,





**Exercise:** Calculate the mesh currents *i*1 and *i*2 in the circuit of shown below.

**Answer:** *i*1 = 23 A, *i*2 = 0 A.



**Problem:** Use mesh analysis to find the current *io* in the circuit below.



**Solution:**

We apply KVL to the three meshes in turn. For mesh 1,

−24 + 10*(i*1 − *i*2*)* + 12*(i*1 − *i*3*)* = 0

or

11*i*1 − 5*i*2 − 6*i*3 = 12 (1)

For mesh 2,

24*i*2 + 4*(i*2 − *i*3*)* + 10*(i*2 − *i*1*)* = 0

or

−5*i*1 + 19*i*2 − 2*i*3 = 0 (2)

For mesh 3,

4*io* + 12*(i*3 − *i*1*)* + 4*(i*3 − *i*2*)* = 0

But at node A, *io* = *i*1 − *i*2, so that

4*(i*1 − *i*2*)* + 12*(i*3 − *i*1*)* + 4*(i*3 − *i*2*)* = 0

or

−*i*1 − *i*2 + 2*i*3 = 0 (3)

In matrix form, Eqs. (1) to (3) become



We obtain the determinants as



= 418 − 0 − 0 − 114 − 22 − 0 = 192





We calculate the mesh currents using Cramer’s rule as



Thus, *io* = *i*1 − *i*2 = 1*.*5 A.

**Exercise:** Using mesh analysis, find *io* in the circuit shown below.

**Answer:** −5 A.

****

**MESH ANALYSIS WITH CURRENT SOURCES**

Applying mesh analysis to circuits containing current sources (dependent or independent) may appear complicated. But it is actually much easier than what we encountered in the previous section, because the presence of the current sources reduces the number of equations. Consider the following two possible cases.

**CASE 1:** **1** When a current source exists only in one mesh: Consider the circuit in Fig. 11, for example. We set *i*2 = −5 A and write a mesh equation for the other mesh in the usual way, that is,

−10 + 4*i*1 + 6*(i*1 − *i*2*)* = 0 \_⇒ *i*1 = −2 A (1)



Figure 11.

Figure: a circuit with current source

**CASE 2:2** When a current source exists between two meshes: Consider the circuit in Fig. 11(a), for example. We create a *supermesh* by excluding the current source and any elements connected in series with it, as shown in Fig. 11(b). Thus,

**A supermesh** results when two meshes have a (dependent or independent) current source in common.





Figure 11: (a) Two meshes having a current source in common, (b) a supermesh, created by excluding the current source.

As shown in Fig. 11(b), we create a supermesh as the periphery of the two meshes and treat it differently. (If a circuit has two or more supermeshes that intersect, they should be combined to form a larger supermesh.) Why treat the supermesh differently? Because mesh analysis applies KVL—which requires that we know the voltage across each branch—and we do not know the voltage across a current source in advance. However, a supermesh must satisfy KVL like any other mesh. Therefore, applying KVL to the supermesh in Fig. 11(b) gives

−20 + 6*i*1 + 10*i*2 + 4*i*2 = 0

or

6*i*1 + 14*i*2 = 20 (2)

We apply KCL to a node in the branch where the two meshes intersect. Applying KCL to node 0 in Fig. 11(a) gives

*i*2 = *i*1 + 6 (3)

Solving Eqs. (2) and (3), we get

*i*1 = −3*.*2 A*, i*2 = 2*.*8 A (4)

Note the following properties of a supermesh:

1. The current source in the supermesh is not completely ignored; it provides the constraint equation necessary to solve for the mesh currents.

2. A supermesh has no current of its own.

3. A supermesh requires the application of both KVL and KCL.

**Problem:** For the circuit below, find *i*1 to *i*4 using mesh analysis.



**Solution:**

Note that meshes 1 and 2 form a supermesh since they have an independent current source in common. Also, meshes 2 and 3 form another supermesh because they have a dependent current source in common. The two supermeshes intersect and form a larger supermesh as shown. Applying KVL to the larger supermesh,

2*i*1 + 4*i*3 + 8*(i*3 − *i*4*)* + 6*i*2 = 0

or

*i*1 + 3*i*2 + 6*i*3 − 4*i*4 = 0 (1)

For the independent current source, we apply KCL to node *P*:

*i*2 = *i*1 + 5 (2)

For the dependent current source, we apply KCL to node *Q*:

*i*2 = *i*3 + 3*io*

But *io* = −*i*4, hence,

*i*2 = *i*3 − 3*i*4 (3)

Applying KVL in mesh 4,

2*i*4 + 8*(i*4 − *i*3*)* + 10 = 0

or

5*i*4 − 4*i*3 = −5 (4)

From Eqs. (1) to (4),

*i*1 = −7*.*5 A*, i*2 = −2*.*5 A*, i*3 = 3*.*93 A*, i*4 = 2*.*143 A

**Exercise:** Use mesh analysis to determine *i*1*, i*2, and *i*3 in Figure shown below.

**Answer:** *i*1 = 3*.*474 A*, i*2 = 0*.*4737 A*, i*3 = 1*.*1052 A.



**DC CIRCUIT THEOREMS**

A linear circuit is one whose output is linearly related (or directly proportional) to its input.

****

Figure: Alinear circuit with input *vs* and output *i*.

**NORTON’S THEOREM:**

states that a linear two-terminal circuit can be replaced by an equivalent circuit consisting of a current source IN in parallel with a resistor RN, where IN is the short-circuit current through the terminals and RN is the input or equivalent resistance at the terminals when the independent sources are turned off.



Figure 11: (a) Original circuit, (b) Norton equivalent circuit.

Thus, the circuit in Fig. 11(a) can be replaced by the one in Fig. 11(b).

The proof of Norton’s theorem will be given in the next section. For now, we are mainly concerned with how to get RN and IN. We find RN in the same way we find RTh. In fact, from what we know about source transformation, the Thevenin and Norton resistances are equal; that is,

RN = RTh

To find the Norton current IN, we determine the short-circuit current flowing from terminal a to b in both circuits in Fig. 11. It is evident that the short-circuit current in Fig. 11(b) is IN. This must be the same short-circuit current from terminal a to b in Fig. 11(a), since the two circuits are equivalent. Thus,

IN = isc

**Steps to determine Norton’s Theorem:**

1. Identify and remove the Load.
2. Short the load terminals and calculate Isc. (IN).
3. Remove all sources by replacing
4. Voltage sources with a short
5. Current sources with an open.
6. If the source has an internal resistance, keep resistance in the circuit.
7. Look in the load terminals and calculate RN
8. Create a parallel circuit consisting of IN and RN and load
9. Calculate the load current or voltage as desired.

Problem: Find the Norton equivalent circuit of the circuit in Figure below



**Solution:**

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figure 12: finding: (a) *RN*, (b) *IN* = *isc*,

We find *RN* in the same way we find *R*Th in the Thevenin equivalent circuit. Set the independent sources equal to zero. This leads to the circuit in Figure 12(a), from which we find *RN*. Thus,

.****

To find *IN*, we short-circuit terminals *a* and *b*, as shown in Fig. 12(b). We ignore the 5Ωresistor because it has been short-circuited. Applying mesh analysis, we obtain



From these equations, we obtain

*i*2 = 1 A = isc= IN

****

Figure: Norton equivalent of the circuit for the given circuit.

**Exercise:** Find the Norton equivalent circuit for the circuit shown below.

**Answer:** RN = 3 Ω, IN = 4.5 A.



 **THEVENIN’S THEOREM**

states that a linear two-terminal circuit can be replaced by an equivalent circuit consisting of a voltage source *V*Th in series with a resistor *R*Th, where *V*Th is the open-circuit voltage at the terminals and *R*Th is the input or equivalent resistance at the terminals when the independent sources are turned off.



Figure 13: Replacing a linear two-terminal circuit by its Thevenin equivalent: (a) original circuit, (b) the Thevenin equivalent circuit.

**Steps to determine Thevenin’s Theorem:**

1. Identify and remove the Load.
2. Open the load terminals and calculate VTh
3. Remove all sources by replacing
4. Voltage sources with a short
5. Current sources with an open.
6. If the source has an internal resistance, keep resistance in the circuit.
7. Look in the load terminals and calculate RTh
8. Create a series circuit consisting of VTh and RTh and load
9. Calculate the load current or voltage as desired.

****





**Problem:** Find the Thevenin equivalent circuit of the circuit shown below, to the left of the terminals *a*-*b*. Then find the current through *RL* = 6*,* 16,and 36Ω.



**Solution:**

We find *R*Th by turning off the 32-V voltage source (replacing it with a short circuit) and the 2-A current source (replacing it with an open circuit). The circuit becomes what is shown in Fig.13(a). Thus,



Figure 13: For Example13: (a) finding *R*Th, (b) finding *V*Th. To find *V*Th, consider the circuit in Fig. 13(b).

To find *V*Th, consider the circuit in Fig.13(b). Applying mesh analysis to the two loops, we obtain

−32 + 4*i*1 + 12*(i*1 − *i*2*)* = 0*, i*2 = −2 A

Solving for *i*1, we get *i*1 = 0*.*5 A. Thus,

*V*Th = 12*(i*1 − *i*2*)* = 12*(*0*.*5 + 2*.*0*)* = 30 V

Alternatively, it is even easier to use nodal analysis. We ignore the 1Ω resistor since no current flows through it. At the top node, KCL gives



or



as obtained before. We could also use source transformation to find *V*Th. The Thevenin equivalent circuit is shown in below circuit. The current through *RL* is







**Exercise:** Using Thevenin’s theorem, find the equivalent circuit to the left of the terminals in the circuits hown below. Then find *i*.

****

**Answer:** *V*Th = 6 V, *R*Th = 3 Ω*, i* = 1*.*5 A.

**SUPERPOSITION THEOREM**

The **superposition** principle states that the voltage across (or current through) an element in a linear circuit is the algebraic sum of the voltages across (or currents

through) that element due to each independent source acting alone.

The principle of superposition helps us to analyze a linear circuit with more than one independent source by calculating the contribution of each independent source separately. However, to apply the superposition principle,

we must keep two things in mind:

1. We consider one independent source at a time while all other independent sources are *turned off*. This implies that we replace every voltage source by 0 V (or a short circuit), and every current source by 0 A (or an open circuit). This way we obtain a simpler and more manageable circuit.
2. Dependent sources are left intact because they are controlled by circuit variables.

**Steps to apply superposition principle:**

1. Turn off all independent sources except one source. Find the output (voltage or current) due to that active source using nodal or

mesh analysis.

2. Repeat step 1 for each of the other independent sources.

3. Find the total contribution by adding algebraically all the contributions due to the independent sources.

**Problem:** Use the superposition theorem to find *v* in the circuit given below.



**Solution:**

****

Figure 14: For Example 4.3: (a) calculating *v*1, (b) calculating *v*2.

Since there are two sources, let

*v* = *v*1 + *v*2

where *v*1 and *v*2 are the contributions due to the 6-V voltage source and the 3-A current source, respectively. To obtain *v*1, we set the current source to zero, as shown in Fig. 14(a). Applying KVL to the loop in Fig. 14(a) gives



Thus,

*v*1 = 4*i*1 = 2 V

We may also use voltage division to get *v*1 by writing



To get *v*2, we set the voltage source to zero, as in Fig. 14(b). Using current division,



Hence,

*v*2 = 4*i*3 = 8 V

And we find

*v* = *v*1 + *v*2 = 2 + 8 = 10 V

**problem:** For the circuit given below, use the superposition theorem to find *i*.

****

**Solution:**

****

In this case, we have three sources.

 Let

*i* = *i*1 + *i*2 + *i*3

where *i*1*, i*2, and *i*3 are due to the 12-V, 24-V, and 3-A sources respectively. To get *i*1, consider the circuit in Fig. (a). Combining 4*\_*(on the right hand side) in series with 8 Ω gives 12 Ω. The 12 Ωin parallel with 4 Ω

gives 12 × 4*/*16 = 3 Ω .Thus,



To get *i*2, consider the circuit in Fig. (b). Applying mesh analysis,

 (1) (2)

Substituting Eq. (2) into Eq. (1) gives

*i*2 = *ib* = −1

To get *i*3, consider the circuit in Fig. (c). Using nodal analysis,

**** (3)

**** (4) Substituting Eq. (4) into Eq. (3) leads to *v*1 = 3 and

****

Thus,

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